AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A method of forming a multilayered circuit board, comprising:

a first circuit forming process of forming a first circuit made of a conductor in a predetermined pattern on a first flat surface of a flat insulating board made of an insulating material, ~~the~~ said insulating board further having a second flat surface approximately parallel to ~~the~~ said first flat surface;

a first circuit embedding process of embedding ~~the~~ said first circuit in ~~the~~ said first insulating board so that ~~the~~ said first surface and ~~the~~ said first circuit have a predetermined surface ~~flatness~~ flatness, and so that ~~the~~ said first surface has a predetermined parallelism with respect to ~~the~~ said second flat surface;

a masking process of forming, on a part of a surface of the embedded first circuit, a mask for forming a pilot hole for a via hole;

an insulating layer forming process of forming an insulating material layer by applying ~~the~~ insulating material as a layer ~~to the~~onto said first flat surface ~~having the mask formed thereon~~and embedded first circuit except ~~the~~ for a part ~~of the surface~~thereof on which ~~the~~ said mask is located;

an insulating material layer flattening process of flattening a surface of ~~the~~ said insulating material layer so that ~~the~~ said surface of the insulating material layer has the surface flatness and the parallelism with respect to ~~the~~ said second flat surface; and

a pilot hole forming process of forming the pilot hole by removing ~~the~~ said mask from ~~the~~ said first circuit with ~~the~~ said insulating material layer ~~being~~ having been flattened.

2. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

$S < 5\mu m$, and

$P < 5\ \mu\ m$,

~~where~~ wherein S is the surface flatness and P is the parallelism.

3. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said first circuit embedding process includes:

a process of heating and maintaining ~~the~~ said insulating material of said insulating board, and ~~the~~ said first ~~circuit~~ circuit, at a predetermined temperature T; and

a process of pressuring the heated and maintained insulating material and first circuit at a predetermined pressure F ~~to the~~toward said second flat surface ~~with~~ to achieve the surface flatness and the parallelism, wherein

$100℃ \leqq T \leqq 200℃$,

$2\times10^6Pa \leqq F \leqq 5\times10^6Pa$, and

$300\times10^6Pa \leqq T\times F \leqq 600\times10^6Pa$.

4. (Currently amended) The method of forming the multilayered circuit board according to claim 1, further comprising:

a via hole forming process of forming the via hole by filling ~~the~~ said pilot hole with ~~the~~ a conductor;

a second circuit forming process of forming a second circuit by applying ~~the~~ a conductor to ~~the~~ a surface of the flattened insulating material layer in a predetermined pattern; and

a second circuit embedding process for embedding ~~the~~ said second circuit in ~~the~~ said flattened insulating material layer so that ~~the~~ a surface of ~~the~~ said flattened insulating material layer and ~~the~~ said second circuit have the surface ~~flatness~~ flatness, and so that ~~the~~ said surface of ~~the~~ said flattened insulating material layer has the parallelism with respect to ~~the~~ said second flat surface.

5. (Currently amended) The method of forming the multilayered circuit board according to claim 4, further comprising

a circuit board multilayering process of successively forming a predetermined number of circuit boards by repeating ~~the~~ said second circuit forming process and ~~the~~ said second circuit embedding process ~~for~~ a predetermined number of times.

6. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said insulating material of said insulating board contains a plastic component.

7. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said conductor is selected from a group including Au, Ag, Cu, Ni, Sn, and Pd.

8. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said conductor is selected from a group including ~~a~~ an Au compound, ~~a~~ an Ag compound, a Cu compound, ~~a~~ an Ni compound, ~~a~~ an Sn compound, and a Pd compound.

9. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said conductor is selected from a group including an alloy mainly containing any of Au, Ag, Cu, Ni, Sn, and Pd.

10. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said conductor is a mixture of an alloy mainly containing any of Au, Ag, Cu, Ni, Sn, and Pd, and an organic compound.

11. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said mask is of a material selected from a group including a compound containing fluorine, a monad, a resin, a polyethylene resin, a polypropylene resin, a vinyl chloride resin, a nylon resin, a sublime compound, and a basic acid compound.

12. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said mask is formed through any of plasma coating, PVD, CVD, PCVD, spraying, and printing.

13. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~the~~ said mask is removed through a scheme selected from a group including plasma etching, spattering, chemical etching, and heating.

14. (Currently amended) The method of forming the multilayered circuit board according to claim 1, wherein

~~in the~~said first circuit forming ~~process, the~~process comprises forming a first circuit that includes a component.

15. (Currently amended) The method of forming the multilayered circuit board according to claim 4, wherein

~~in the~~said second circuit forming ~~process, the~~process comprises forming a second circuit that includes a component.

Claims 16-17 (Cancelled)

18. (New) The method of forming the multilayered circuit board according to claim 6, wherein

said insulating material of said insulating layer contains a plastic component.

19. (New) The method of forming the multilayered circuit board according to claim 1, wherein

said insulating material of said insulating layer contains a plastic component.